PANYA TECHNOLOGIES

Technology to Live…

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ARM CORTEX-M3 SYSTEM DESIGN

OBJECTIVES

This course takes an in depth look at the considerations you will need to take into account when designing a system containing a Cortex-M3 processor core

It is aimed at:

Software engineers who not only want to obtain details of how to write software to run on the Cortex-M3, but also wish to obtain an understanding of hardware design issues Hardware engineers who need to understand how to design Cortex-M3 based systems, but also wish to obtain an understanding of the issues of writing software to run on that system. A basic understanding of microprocessors and microcontrollers is recommended. A basic understanding of digital logic or hardware / ASIC design issues would be useful but not essential. A basic understanding of assembler or C programming would b useful but not essential. A basic awareness ARM cores is useful but not essential.

ARM Cortex-M3 INTRODUCTION

- Programmer's model
- Fixed memory map
- Privilege, modes and stacks
- Memory Protection Unit
- Interrupt handling
- Nested Vectored Interrupt Controller [NVIC]
- Power management
- Debug

ARM Cortex-M3 CORE

- Data path and pipeline
- Write buffer
- Bit-banding
- System timer
- State, privilege and stacks
- System control bloc

THUMB-2 INSTRUCTION SET

- Data processing instructions
- Branch and control flow instructions
- Memory access instructions
- Exception generating instructions
- If…then conditional blocks
- Exclusive load and store instructions
- Accessing special registers
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- Memory barriers and synchronization
- Workbook : introductory tutorial for Cortex-M3

INTERRUPTS

- Interrupt entry / exit, timing diagrams
- Tail chaining
- Interrupt response, pre-emption
- Interrupt prioritization

- Interrupt implementation configurability, impact on core size

EXCEPTIONS

- Exception behavior, exception return
- Non-maskable exceptions
- Privilege, modes and stacks
- Fault escalation
- Vector table

MEMORY TYPES

- Memory types, restriction regarding load / store multiple
- Device and normal memory ordering
- Access order
- Memory barriers

MEMORY PROTECTION UNIT

- Memory protection overview, ARM v7 PMSA
- Cortex-M3 MPU and bus faults
- Region overview, memory type and access control, sub-regions

Cortex-M3

- Placing code, data, stack and heap in the memory map,
- scatterloading
- Tailoring the C library to your target
- Reset and initialisation
- Building and debugging your image
- Long branch veneers
- Workbook : Retargeting the standard C library functions,
- handling interrupts

INVASIVE DEBUG

- Cortex-M3 debug features
- Monitor mode
- Flash patch and breakpoint features
- Data watchpoint and trace
- DWT registers
- AHB-Access Port

NON-INVASIVE DEBUG

- Basic ETM operation
- ITM stimulus port registers
- DWT trace packets
- Time-stamping packets
- TPIU components
- Serial Wire connection

C/C++ COMPILER HINTS AND TIPS FOR Cortex-M3

- ARM compiler optimizations
- Mixing C/C++ and assembly
- Coding with ARM compiler
- Measuring stack usage
- Local and global data issues, alignment of structures

AMBA3.0 INTERCONNECT SPECIFICATION

- Purpose of this specification
- Example of SoC based on AMBA specification
- Differences between AMBA2.0 and AMBA3.0

AHB - ADVANCED HIGH PERFORMANCE BUS

- Centralized address decoding
- Address gating logic
- Arbitration, bus parking
- Single-data transactions
- Sequential transfers
- Retry response
- Split response
- AHB-lite specification

APB - ADVANCED PERIPHERAL BUS

- Read timing diagram
- Write timing diagram
- Operation of the AHB-to-APB bridge
- APB3.0 new features

AHB CORTEX-M3 HARDWARE IMPLEMENTATION

- Clocking and reset
- Bus interfaces , AMBA-3 compliance
- Debug interface, AHB-AP programming interface, ITM, ETM Connection to the TPIU